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Magazine

2002 October Go

Current Issue
Subscriptions
Media Information
Editorial Policy
Contact us

Removing the GaAs via hole etch process bottleneck

Increasing the speed of GaAs backside via etching is the current mission for manufacturers of dry etch tools. Young Cho and Jim Thomas of equipment manufacturer Tegal explore the new problems that high etching speeds bring, and suggest strategies for how they can be solved.

GaAs backside via etching is one of the most critical processes in the manufacture of GaAs MMICS. Contacts through via holes provide low inductance grounds that are critical to the performance of FETs and MMICs (Williams). Since the process was initially developed, much effort has been invested in increasing the etch rate and therefore reducing both the process time and the manufacturing costs.

GaAs backside via etching has a reputation as a bottleneck process in MMIC manufacturing. The drive to eliminate this bottleneck has stimulated great competition between dry-etch equipment manufacturers to increase the etch rates of their tools.

However, the strong demand for a high-rate backside via etch has not yet been fully satisfied in the GaAs device industry. GaAs provides a number of performance advan-tages for high-speed devices, but the complicated material properties of compound semiconductors require comprehensive work on process development.

At Tegal we have carried out a project to develop a high-rate GaAs via etch, exploring how process parameters such as chamber pressure and wafer temperature affect the etch rate and the factors that need to be considered in order to ensure defect-free vias.

A new process window

The etching experiments described below were carried out on 4 inch GaAs wafers using Tegal's HRe (high-density reflected electron) plasma-etch tool. The plasma-etch process involves introducing a gas containing an element, in this case chlorine, that is reactive with the material to be etched. A plasma is struck in the Cl gas mixture, forming charged Cl radicals that are accelerated towards the substrate by the application of a DC bias. These radicals react with the GaAs, forming volatile gaseous $AsCl_3$ and $GaCl_3$ species which are pumped away.

Using a DC bias means that the etchant radicals are accelerated vertically down onto the substrate, so features with high aspect ratios such as via holes can be etched.

Links

Author
Young Cho and Jim Thomas

Maintaining the plasma density and uniformity at high pressure is very important for achieving a high etch rate. A high pressure means that there is an abundance of the reactive species available. Energetic free electrons within the plasma impact with the heavier Cl-containing molecules, breaking the chemical bonds and thereby releasing charged Cl radicals for etching.

It is well known that conventional reactive ion etch and inductively coupled plasma tools have difficulty sustaining a high-density plasma at chamber pressures over 20 mTorr, because the mean free path of electrons reduces as the pressure rises. In the HRe, permanent magnets at the top of the chamber and at its sidewalls reflect free electrons back into the plasma, making it possible to maintain a high plasma density at high chamber pressure. This provides a new window of process parameters to explore.

For the development of a high etch rate process in the HRe, a 13.56 MHz generator was used for plasma generation, and 450 kHz was chosen as the bias power frequency. The GaAs wafers were coated with an AZ4620 photoresist etch mask and patterned with 50 µm diameter holes more than 100 µm apart. RS/1 data management and analysis software from BBN Corporation was used for designing the experiment and analyzing the results.

Performance under pressure

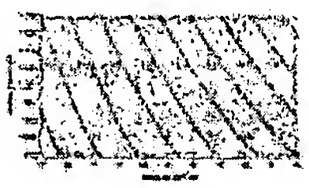

Figure 1

Figure 1 shows the GaAs etch rate as a function of the source power and chamber pressure. The results show that pressure has a much stronger influence on GaAs etch rate than the source power. The etch rate also shows a linear increase with increasing pressure. This implies that the GaAs etch rate is limited by the amount of chlorine radicals present. Therefore the key to achieving a high etch rate is to provide sufficient reactant at a high chamber pressure. The highest etch rate achieved was more than 10 µm/min at a chamber pressure of 35 mTorr.

Figure 2 shows the etch selectivity to photoresist for the same process parameters as figure 1. A maximum selectivity of 27:1 was achieved at the highest chamber pressure. The etch rate of the photoresist is dominated by the DC bias and the energy of the etchant ions. The etch rate for GaAs is largely chemically dependent so it increases at higher pressures. The photoresist etch rate therefore remains more stable than that of GaAs as the pressure rises, improving the etch selectivity.

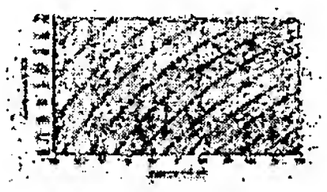

Figure 2

Magazine

2002 October Go

Current Issue
Subscriptions
Media Information
Editorial Policy
Contact us

Links

Author

Young Cho and Jim Thomas

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Etch stop and pillar formation

Within the process window for obtaining high etch rates, the elimination of defects such as pillar formation and the possibility of etch stop caused by polymer build-up become the critical issues. Many laboratories have already investigated the relationship between pillar formation and the wafer condition or the process parameters (Kiriakidis *et al.*, Nam *et al.*). Polymers of various types are formed during etching as a result of reactions between the chlorine-based etchant, gallium and the photoresist mask. The amount of polymer generated rises with etch rate, and excessive polymer generation can slow and eventually stop etching. Etch stop can be avoided by controlling the wafer temperature and optimizing the bias power. Heavy polymer deposition and pillar defects in GaAs via holes are shown in figures 3a and 3b.

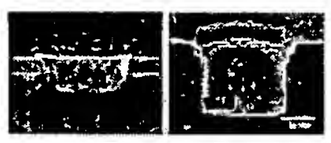


Figure 3

Pillar formation is a well known phenomenon, but it is not fully understood and it is a difficult problem to solve. Carbon-rich impurities on the wafer surface or within the epitaxial layer can cause pillars to form, although improving the pre-etch wafer-processing steps makes it less likely. The incorrect combination of etch-process variables such as chamber pressure and DC bias can also result in pillar formation.

The effects of wafer temperature have also been investigated in Tegal's development laboratory and found to have a major impact on pillar formation. Figures 5a and 5b show the results of optical surface-profiler scans on two GaAs samples at different temperatures. The temperatures of the samples in 5a and 5b are 0 and -20 °C respectively. The average surface roughness (Ra) is 504.8 nm for 5a and 403.6 nm for 5b.

Figure 4

The difference in Ra at the two temperatures stems from the different melting temperatures of the two major reaction products formed during etching. The melting point of $GaCl_3$ (77.9 °C) is much higher than that of $AsCl_3$ (-16 °C). As the temperature rises towards 77.9 °C, the liquid $AsCl_3$ becomes increasingly volatile while the solid $GaCl_3$ remains more stable. The disparity in the materials' volatility causes roughening of the surface during etching, which can eventually induce the pillar-shaped defects.

Therefore the surface roughness can be minimized by reducing the difference in

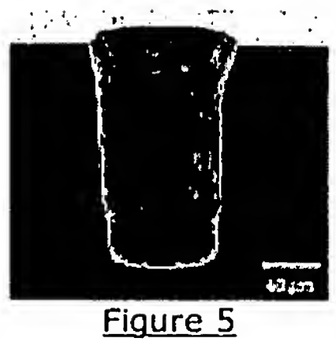


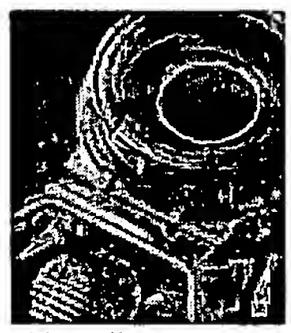
Figure 5

volatility between the by-products of the etching reaction. This can be achieved by etching at a low temperature or by changing the process in some way to improve the removal of $GaCl_3$. Experiments have shown that as the wafer temperature decreases, pillar formation is eventually eliminated near -20 °C.

Beyond 10 µm/min

The pressure of the process chamber has turned out to be the most important process parameter for achieving high GaAs etch rates, with the etch rate showing a very proportional increase with chamber pressure. As the GaAs etch rate increases, defect control becomes critical. A large amount of polymer byproducts can induce etch-stop problems and the high etch rate makes pillar formation more likely. The optimized GaAs etch results are shown in figure 5. An etch rate of more than 10 µm/min can be achieved without etch stop or pillar formation. The test results also revealed the possibility of increasing GaAs backside via etch rates beyond 10 µm/min.

Device pattern sizes are constantly reducing and even higher GaAs etch rates for smaller vias will be required in the future. This will ensure that the competition between dry-etch tool vendors for the higher GaAs etch rate process will continue as long as backside processes are necessary in MMIC manufacturing. GaAs etch rates have improved very rapidly and 20 µm/min can be expected in the near future.



Tegal's reactor

Further reading

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About the author

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